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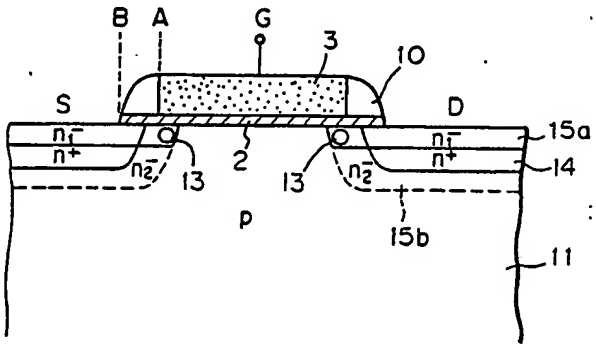
(54) Semiconductor device.

(57) A semiconductor device has a gate electrode (3) formed on a semiconductor substrate (11), and a source region (S) and a drain region (D) formed in the semiconductor substrate. The source and drain regions each comprise a first impurity region (15a), doped with impurity of opposite conductivity type to that of the semiconductor substrate and formed at a portion adjacent an edge (A) of the gate electrode. A second impurity region (15b) doped with impurity of opposite conductivity type to the semiconductor substrate is formed at a portion under the first impurity region, the impurity of the second impurity region having a diffusion coefficient larger than that of the impurity of the first impurity region. A third impurity region (14) doped with impurity of opposite conductivity type to the semiconductor substrate, is formed at a portion spaced from the edge of the gate electrode, the third impurity region having a higher concentration than that of the first and second impurity regions, and the impurity of the third impurity region having a diffusion coefficient smaller than that of the second impurity region. By constructing the device in this manner, the channel hot-electron and avalanche hot-electron phenomena are reduced, and the mutual conductance is increased.

Fig. 5A



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SEMICONDUCTOR DEVICE

This invention relates to a semiconductor device, and more particularly to a semiconductor device wherein source and drain regions having three regions formed by three different types of impurity doping steps are formed to prevent the occurrence of hot electrons which otherwise cause deterioration of the performance of the device.

With the miniaturisation of semiconductor devices, the length of the gate electrode of a MIS FET has been shortened. The supply voltage is generally maintained at 5 V, and there is no tendency to lower this voltage. Hence, particularly in an n-channel MIS transistor, the drain electric field is larger than in a conventional device, and some of the electrons accelerated by the increased electric field are injected into the gate insulating film. This is well known as a channel hot-electron phenomenon. Furthermore, some of the electrons generated by the impact ionisation are injected into the gate insulating film and change the characteristic of the MIS transistor. This is well known as an avalanche hot-electron phenomomen.

In order to solve the problem of the hot electron phenomena, a double diffused drain (DDD) structure and a lightly doped drain (LDD) structure have been proposed, in which the electric field is not concentrated in the DDD structure, and the hot electron phenomenon is therefore reduced. However, in the DDD structure the effective channel length is decreased and a punch-through phenomenon is therefore generated. Furthermore, problems of deterioration in the mutual conductance (g_m) and in the breakdown voltage arise.

On the other hand, although the LDD structure has an effect on the channel hot-electron phenomenon, it has little effect on the avalanche hot-electron phenomenon in which electrons generated at a deeper portion of the substrate due to the high electric field strength are accelerated so that the electrons are moved to the gate electrode through the gate insulating film. In addition, in the LDD structure deterioration of the mutual conductance also occurs.

Accordingly, an object of the present invention is to provide a semiconductor device, particularly a MIS FET, wherein channel hot-electron and avalanche hot-electron phenomena are decreased.

Another object of the present invention is to provide a semiconductor device wherein the mutual conductance (g_m) thereof is improved.

According to the invention there is provided a semiconductor device having a gate electrode formed on a semiconductor substrate and source and drain regions formed in the semiconductor substrate, characterised in that the source and drain regions each comprise a first impurity region doped with impurity of opposite conductivity type to that of the semiconductor substrate and formed at a portion adjacent an edge of the gate electrode; a second impurity region doped with impurity of opposite conductivity type to the semiconductor substrate and formed at a portion under the first impurity region, the impurity of the second impurity region having a diffusion coefficient larger than that of the impurity of the first impurity region; and a third impurity region doped with impurity of opposite conductivity type to the semiconductor substrate and formed at a portion spaced from the edge of the gate electrode, the third impurity region having a higher concentration than that of the first and second impurity regions and the impurity of the third impurity region having a diffusion coefficient smaller than that of the second impurity region.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1A is a cross-sectional view of an example of a conventional DDD structure;

Figure 1B is an equivalent circuit of the structure of Figure 1A;

Figures 2, 3 and 4 are cross-sectional views of respective examples of conventional LDD structures;

Figure 5A is a cross-sectional view of an example of an n-channel MIS FET according to the present invention;

Figure 5B is an equivalent circuit of the MIS FET of Figure 5A; and

Figures 6A to 6D and Figures 7A to 7D are cross-sectional views for explaining two production processes for forming devices according to the invention.

Before describing a preferred embodiment of the present invention, the related art will be explained in more detail with reference to the drawings.

Figure 1A is a cross-sectional view of a conventional example of a DDD structure, wherein an insulating film 2 and a gate electrode 3 are provided on a p-type semiconductor substrate 1. In the substrate 1 an n^+ region 4 and an n^- region 5 are formed by doping, for example, arsenic ions (As^+) and phosphorus ions (P^+), followed by annealing. Since the diffusion coefficient of phosphorus is considerably larger than that of arsenic, a double diffused drain (DDD) region, i.e. an n^+ region (As^+) and an n^- region (P^+), is formed. The structure formed before the DDD structure was formed had only the n^+ region 4, wherein As^+ was diffused, so that a step-junction was formed. Hence, in the prior structure, an electric field concentrated at a portion 6 in the n^+ region 4 where the step-junction was formed, and this led to the problem of the occurrence of the hot-electron phenomenon as mentioned above.

Therefore, by forming the above mentioned n^- region (P^+) 5 of the DDD structure in such a manner that the n^- region (P^+) 5 covers the n^+ region 4, a graded junction formed by the diffusion of a P^+ electric field is shifted to a portion 7 in the n^- region. Consequently, the concentration of an electric field in the portion 7 is considerably decreased compared to that in the portion 6.

However, the DDD structure has an effective channel length (C2) shorter than that (C1) of a prior structure not having an n^- region, as shown in Figure 1A. Consequently, in the DDD structure a punch-through phenomenon often occurs between the source and drain region. Further, in the DDD structure, the properties of the FET are determined by the concentration of P^+ in the n^- type region 5. If the concentration of P^+ is low, parasitic series resistance is generated, as shown by reference 8 in Figure 1A.

An equivalent circuit of the device of Figure 1A is shown in Figure 1B. Thus, it can be seen that if the concentration of P^+ is low, the mutual conductance (g_m) of the device cannot be increased. On the other hand, if the concentration of P^+ is high, the breakdown voltage is lowered.

Referring to Figure 2, a lightly-doped drain (LDD) structure is shown in which a gate insulating film 2, a gate electrode 3, and a side wall 10 are formed on a p-type semiconductor substrate 1. In the substrate 1 an n^- region 5 and an n^+ region 4 formed by doping As^+ and subsequent annealing are provided. In the formation process of the n^- and n^+ regions, As^+ having a low concentration is doped into the substrate 1 to form the n^- region 5, and As^+ having a high concentration is doped therein to form an n^+ region 4. Since the diffusion depth (x_j) of the doped impurities is determined by the root of the concentration (C) thereof, i.e. $x_j \propto \sqrt{C}$, an LDD structure as shown in Figure 2 is obtained. The LDD structure can prevent occurrence of channel hot electrons at a portion 11 in Figure 2. However, the LDD structure cannot prevent the occurrence of avalanche hot electrons which are generated at a deeper portion 12 of the substrate 1 due to the high electric field strength, and accelerated to move into the gate electrode 3 through the gage insulating film 2. Furthermore, deterioration of the mutual conductance (g_m) occurs as in the DDD structure.

Figure 3 shows a semiconductor device as disclosed in Japanese Unexamined Patent Publication (Kokai) No. 60-136376. This device (Hitachi structure) has an n^+ region 4, an n_1^- region 5a and an n_2^- region 5b in the source and drain regions. Each region is produced by a process wherein P^+ is doped to a dosage of 1×10^{13} cm^{-2} using a polycrystalline layer of a gate electrode 3 formed on a gate insulating film 2 as a mask, side walls of SiO_2 are formed so that the gate electrode 3 is sandwiched therebetween, P^+ doped to a dosage of 1×10^{15} cm^{-2} using the gate electrode 3 and the side walls 10 as a mask, P^+ is doped portions are annealed while the doped P^+ is diffused so that the n_1^- region 5a (P^+ doped to a dosage of 1×10^{13} cm^{-2}) and n_2 region 5b (P^+ doped to a dosage of 1×10^{15} cm^{-2}) are formed, As^+ is doped to a dosage of 5×10^{15} cm^{-2} using the gate electrode 3 and the side walls 10 as a mask, and the n^+ region 4 is formed by annealing the As^+ doped portion.

Since the n_1^- region 5a is formed by doping P^+, which has a large diffusion coefficient, into the substrate 1, the distance C3 between the edges of the n_1^- regions 5a, i.e. the channel length, becomes short and the above-mentioned punch-through phenomenon occurs. Further, as explained for the DDD structure, the Hitachi structure is subjected to a resistance due to the diffused n_1^- region 5a, so that the mutual conductance (g_m) is lowered. These disadvantages in the Hitachi structure become greater as the semiconductor device becomes smaller.

Figure 4 shows a semiconductor device disclosed at a Symposium on VLSI Technology, 14 to 16 May, 1985. This device (Toshiba structure) also has three regions, i.e. n_1^-, n_2^-, and n^+ regions.

Each region is produced by a process wherein P^+ and As^+ are doped using a gate electrode 3 as a mask, and P^+ and As^+ doped portions are annealed to form the n_2^- region 5b and n_1^- region 5a, respectively, side walls 10 are formed, As^+ is doped using the gate electrode 3 and the side walls 10 as a mask, and the second As^+ doped portion is annealed to form the n^+ region 4. Since the n_2^- region is formed by annealing the P^+ doped portion, as explained for the Hitachi structure, the Toshiba structure also has the disadvantage of the occurrence of a punch-through phenomenon, and the mutual conductance (g_m) becomes small.

Preferred embodiments of the present invention will now be described.

Figure 5A shows a cross-sectional view for explaining an example of an n-channel MIS FET according to the invention. As shown in Figure 5A, a source (S) region and a drain (D) region in a P-type semiconductor substrate or p-type well 11 each consist of an n_1^- region 15a, an n_2^- region 15b, and an n^+ region 14. An insulating film 2 of, for example, SiO_2, a gate electrode 3 of polycrystalline silicon, and side walls 10 of an insulating material are provided on the semiconductor substrate 11. The n_1^- region 15a is formed by doping impurities having a low concentration from outside the edge A of the gate electrode 3.

On the other hand, the n_2^- region 15b and the n^+ region 14 are formed by doping impurities having a low and a high concentration, respectively, from outside the edges B of the side walls 10. The diffusion coefficient of impurities doped in the n_2^- region is larger than that of impurities doped in the n_1^- and n^+ regions. Although the electric field is concentrated in portions 13 lying in both the n_1^- region 15a and the n_2^- region 15b, the electric field concentration is reduced due to the graded junction of the n_2^- region. This gives an improvement in the deterioration of the properties by two orders, compared with the previous example wherein the hot-electron phenomenon could not be avoided. Furthermore, since the n_2^- region has a graded junction, the depletion layer is expanded and thus the stray capacitance of the source and drain regions is reduced and the switching speed of the device can be increased.

Resistance in the structure is shown in Figure 5B. Namely, the resistance in, for example, the source region, which is generated by the n_1^- and n_2^- regions is the total resistance in the n_1^- and n_2^- regions connected in parallel with each other (not in series) and is reduced, thus allowing an increase in the mutual conductance (g_m).

Processes for producing an embodiment of the invention will now be described with reference to Figures 6A to 6D and Figures 7A to 7D respectively.

As shown in Figure 6A, p-type channel cut regions 16, a field insulating film 12 of, for example, SiO_2, and a gate insulating film 2 of, for example, SiO_2, are formed on a p-type semiconductor substrate 11 which has an impurity concentration of 10^{15} -10^{16} cm^{-3}, and then a gate electrode 3 having a thickness of 2000 to 5000 Å is formed. The gate electrode 3 is made of polycrystalline silicon, a high melting point metal or a high melting point metalsilicide, etc. Then, As^+ is doped to a dosage of 1×10^{13} to 1×10^{15} cm^{-2} at an accelerating energy of 60 to 120 KeV, so that the first lightly-doped n^- regions, i.e. n_1^- regions 15a are formed.

Then, as shown in Figure 6B, an insulating layer 17 having a thickness of 500 to 5000 Å is formed on the obtained structure. Then insulating layer is made of SiO_2 or Si_3N_4 formed by a chemical vapour deposition (CVD) process, etc.

Then, the insulating layer 17 of, for example, CVD-SiO_2, is entirely removed by a reactive ion etching (RIE) process using CHF_3 gas or a mixed gas of CHF_3 and CF_4 under a pressure of 0.1 to 0.2 torr so that side walls 10a are formed in such a manner that they sandwich the gate electrode 3.

Then, as shown in Figure 6C, P^+ having a larger diffusion coefficient than the As^+ is doped to a dosage of 1×10^{13} to 1×10^{15} cm^{-2} at an accelerating energy of 60 to 80 KeV to form a second lightly-doped n^- region, i.e. the n_2^- region 15b, and As^+ is doped to a dosage of 3×10^{15} to 5×10^{15} cm^{-2} at an accelerating energy of 60 to 120 KeV to form a heavily-doped or high-concentration n^+ region 14. The obtained structure is then annealed at a temperature of 900°C to 1100°C in an inert gas atmosphere.

The n_2^- region has a graded junction formed between the n_2^- region and the substrate 1. The graded junction surface formed between the n_2^- region 15b and the substrate 11 forms a surface substantially tangential to a junction surface formed between the n_1^- region 15a and the substrate 11.

Then, as shown in Figure 6D, an insulating layer 20 of, for example, phospho-silicate glass (PSG), boron silicate glass (BSG), etc. is formed, and an aluminium source drawing electrode 21a, an aluminium gate drawing electrode 21b, and an aluminium drain drawing electrode 21C are formed by a usual process. In this manner, a first embodiment of the present invention is produced.

A process for producing a second embodiment of the present invention will now be described. As shown in Figure 7A p-type channel cut regions 16, a field insulating film 2 and a gate insulating film 2 are formed on a p-type semiconductor substrate 11. A gate electrode 3 having a thickness of 2000 to 5000Å and a width longer than the width of the gate electrode in the first embodiment described above is then formed, using a mask 22 of CVD SiO_2 having a thickness of 500 to 2000 Å. The material of the gate electrode is the same as that used in the first embodiment. P^+ is then doped to a dosage of 1×10^{13} to 1×10^{15} cm^{-2} at an accelerating energy of 60 to 80 KeV to form a lightly-doped n_2^- region 15b. Then As^+ is doped to a dosage of 3×10^{15} to 5×10^{15} cm^{-2} at an accelerating energy of 60 to 120 KeV to form a heavily-doped or high concentration n^+ region 14.

Then, as shown in Figure 7B, both sides of the gate electrode 3 are removed by a side plasma etching process using a mixed gas of CF_4 and O_2 (5%) in a polycrystalline silicon gate electrode so that a width of 1000 to 4000 Å is removed from each side thereof.

Then, as shown in Figure 7C, the mask 22 of CVD SiO_2 is removed and As^+ is doped to a dosage of 1×10^{13} to 1×10^{15} cm^{-2} at an accelerating energy of 60 to 120 KeV to form a lightly-doped n_1^- region 15a. An annealing process is then carried out at a temperature of 900°C to 1100°C in an inert gas atmosphere.

Then, as shown in Figure 7D, an insulating layer 20 and aluminium electrodes 21a, 21b, and 21c are formed as described in the first embodiment. A second embodiment of the invention is thereby produced.

Claims

1. A semiconductor device having a gate electrode (3) formed on a semiconductor substrate (11), and source (S) and drain (D) regions formed in the semiconductor substrate, characterised in that the source and drain regions each comprise a first impurity region (15a) doped with impurity of opposite conductivity type to that of the semiconductor substrate and formed at a portion adjacent an edge (A) of the gate electrode; a second impurity region (15b) doped with impurity of opposite conductivity type to the semiconductor substrate and formed at a portion under the first impurity region, the impurity of the second impurity region having a diffusion coefficient larger than that of the impurity of the first impurity region; and a third impurity region (14) doped with impurity of opposite conductivity type to the semiconductor substrate and formed at a portion spaced from the edge of the gate electrode, the third impurity region having a higher concentration than that of the first and second impurity regions and the impurity of the third impurity region having a diffusion coefficient smaller than that of the second impurity region.

2. A device according to claim 1, characterised in that the impurity in the first impurity region (15a) is arsenic.

3. A device according to claim 2, characterised in that the arsenic ions are doped into the semiconductor substrate (11) to a dosage of 1×10^{13} to 1×10^{15} cm^{-2} and at an accelerating energy of 60 to 120 KeV.

4. A device according to any preceding claim, characterised in that the impurity in the second impurity region (15b) is phosphorus.

5. A device according to claim 4, characterised in that the phosphorus ions are doped into the semiconductor substrate (11) to a dosage of 1×10^{13} to 1×10^{15} cm^{-2} and at an accelerating energy of 60 to 80 KeV.

6. A device according to any preceding claim, characterised in that the impurity in the third impurity region (14) is arsenic.

7. A device according to claim 6, characterised in that the arsenic ions are doped into the semiconductor substrate (11) to a dosage of 3×10^{15} to 5×10^{15} cm^{-2} and at an accelerating energy of 60 to 120 KeV.

8. A device according to any preceding claim, characterised in that the spacing from the edge of the gate electrode (3) is determined by the width of a side wall (10) alongside the gate electrode.

9. A device according to any preceding claim, characterised in that a junction surface formed between the first impurity region (15a) and the semiconductor substrate (11) is substantially tangential to a junction surface formed between the second impurity region (15b) and the semiconductor substrate at edges of the source and drain regions adjacent the edges of the gate electrode (3).

Fig. 1A

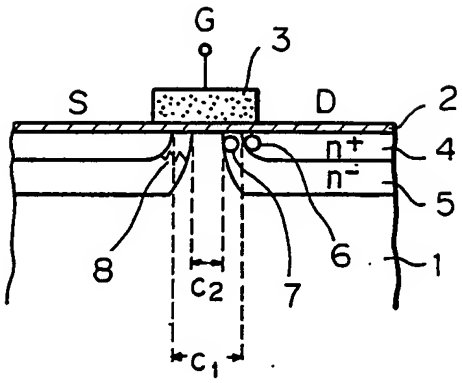

Fig. 1B

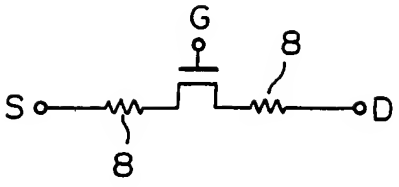

Fig. 2

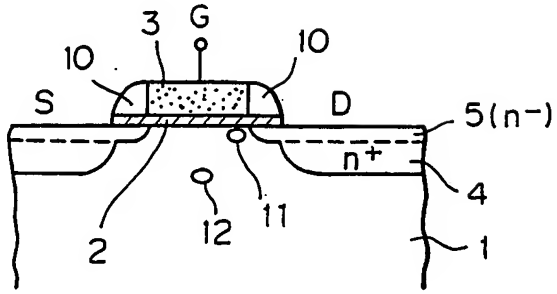

Fig. 3

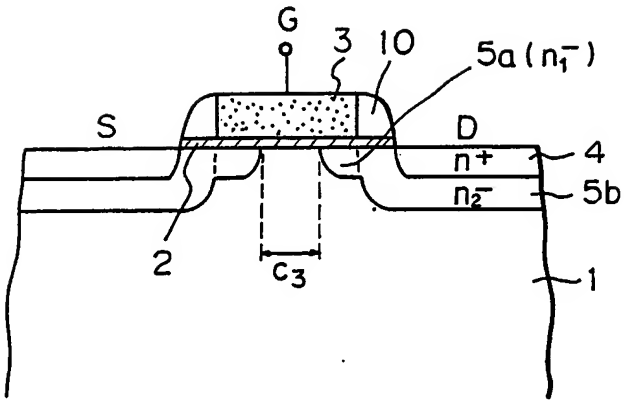

Fig. 4

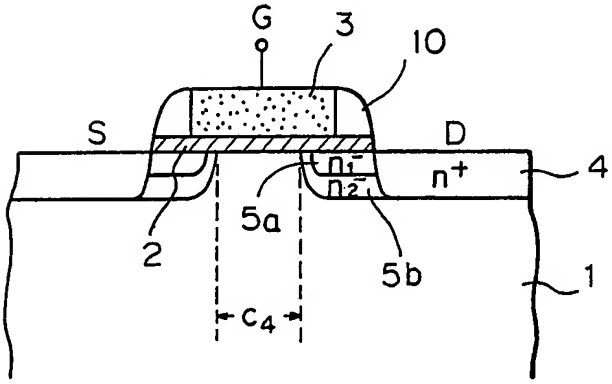

Fig. 5A

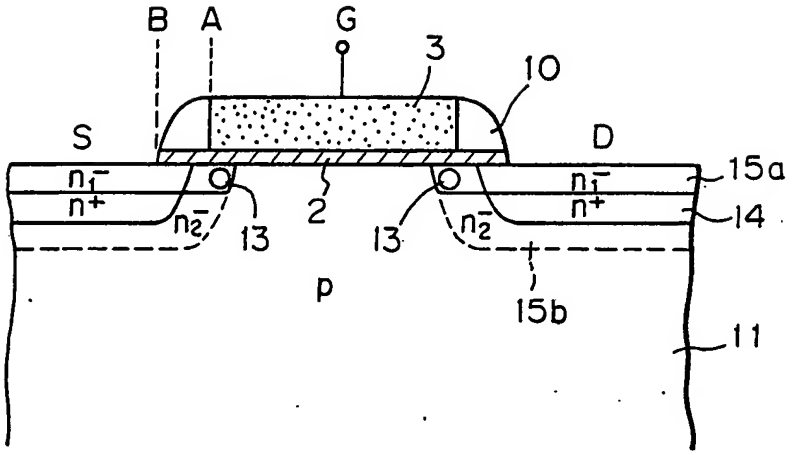

Fig. 5B

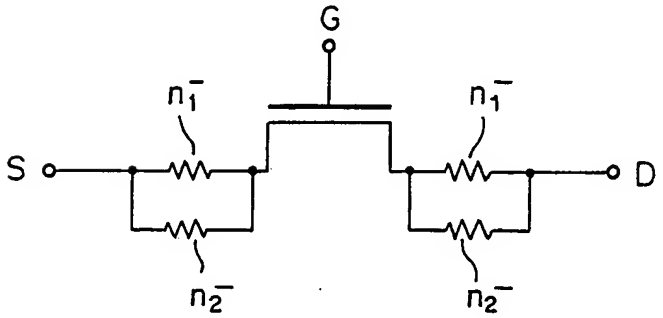

Fig.6A

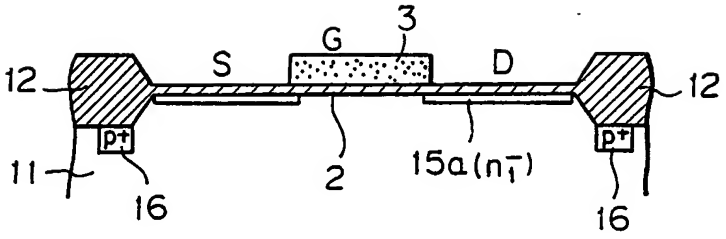

Fig.6B

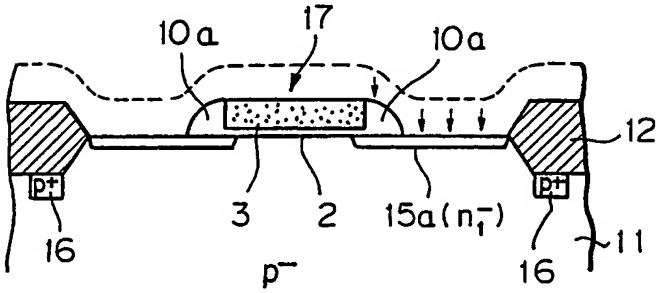

Fig.6C

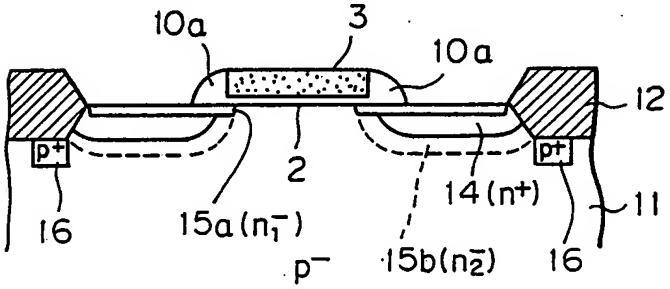

Fig.6D

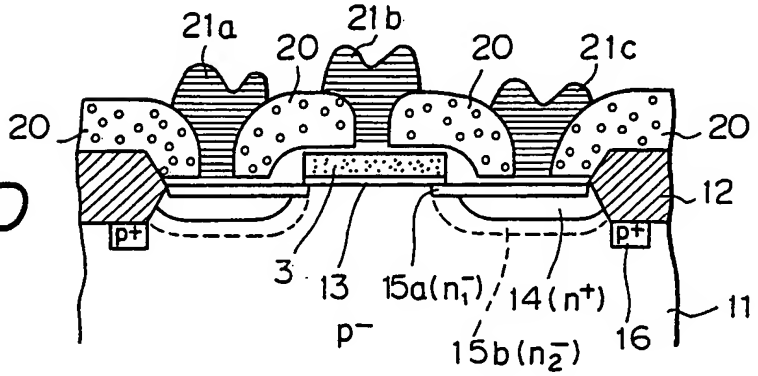

Fig. 7A

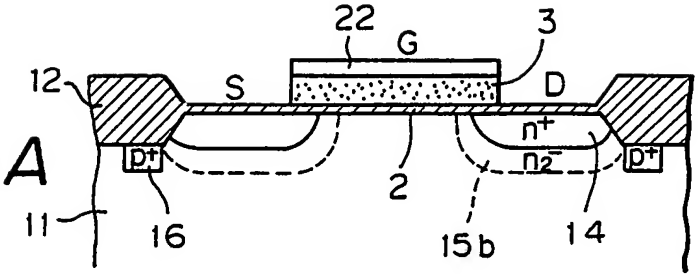

Fig. 7B

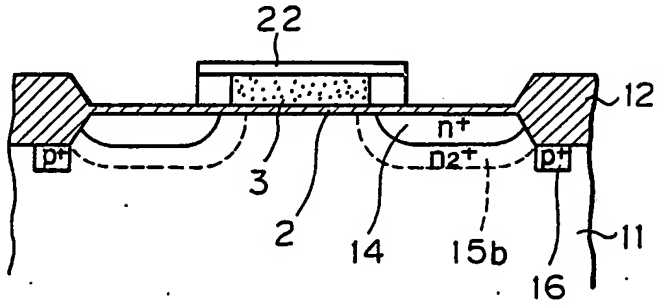

Fig. 7C

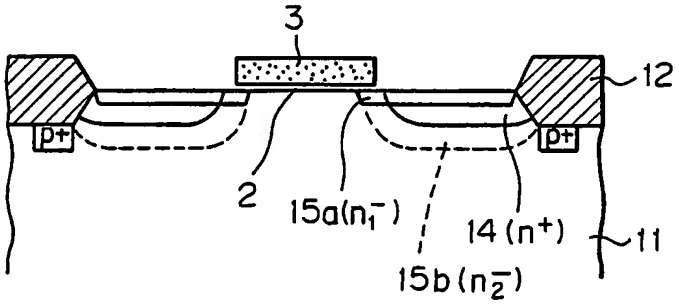

Fig. 7D